On page 47, line 9, delete the first "left" and substitute --right--.

On page 49, line 22, delete "primay" and substitute --primary--.

On page 54, line 13, delete "70" and substitute --69--.

On page 56, line 2, delete "Figurell" and substitute --Figure 11--.

On page 60, line 10, after "147" insert --A, B--.

IN THE CLAIMS:

Kindly **cancel** claims 1-150, without prejudice.

Kindly **add** the following claims:

-- 151. A method of controlling a memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:

providing first block size information to the memory device, wherein the first block size information defines a first amount of data to be input by the memory device in response to a write request; and

issuing a first write request to the memory device, wherein in response to the first write request the memory device inputs the first amount of data corresponding to the first block size information.

152. The method of claim 151 wherein the memory device inputs the first amount of data synchronously with respect to an external clock signal.

153. The method of claim 151 further including:

providing second block size information to the memory device, wherein the second block size information defines a second amount of data to be input by the memory device in response to a write request; and

issuing the second write request to the memory device, wherein in response to the second write request, the memory device inputs the amount of data corresponding to the second block size information.

154. The method of claim 151 wherein the first block size information and the first write request are included in a request packet.

155. The method of claim 154 wherein the first block size information and the first write request are included in the same request packet.

156. The method of claim 151 further including providing the amount of data corresponding to the first block size information to the memory device.

157. The method of claim 156 wherein the data is provided to the memory device after a delay time transpires.

158. The method of claim 156 wherein the delay time is representative of a number of clock cycles of a clock signal.

159. The method of claim 151 wherein the first block size information is a binary representation of the amount of data to be input in response to the first write request.

160. The method of claim 151 wherein the first amount of data corresponding to the first block size information is input synchronously during a plurality of clock cycles of the external clock signal.

161. A method of operation of a memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:

receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be input by the memory device in response to a write request;

receiving a first write request from the bus controller; and

inputting the first amount of data corresponding to the first block size information in response to the first write request.

162. The method of claim 161 wherein the data corresponding to the first block size information is sampled synchronously with respect to the external clock signal.

163. The method of claim 161 further including:

receiving second block size information, wherein the second block size information defines a second amount of data to be input in response to a second write request;

receiving a second write request from the bus controller; and

inputting the amount of data corresponding to the second block size information, in response to the second write request.

164. The method of claim 161 wherein the first block size information and the first write request are included in a request packet.

165. The method of claim 164 wherein the first block size information and the first write request are included in the same request packet.

166. The method of claim 161 wherein the first block size information is a binary representation of the first amount of data to be input in response to the first write request.

167. The method of claim 161 wherein the first amount of data corresponding to the first block size information is input

synchronously during a plurality of clock cycles of an external clock signal.

168. The method of claim 161 further including generating an internal clock signal using a delay locked loop and an external clock signal wherein the first amount of data corresponding to the first block size information is input synchronously with respect to the internal clock signal.

169. The method of claim 161 further including generating first and second internal clock signals using clock generation circuitry and an external clock signal wherein the first amount of data corresponding to the first block size information is input synchronously with respect to the first and second internal clock signals.

170. The method of claim 169 wherein the first and second internal clock signals are generated by a delay lock loop.

171. A method of operation of an integrated circuit, wherein the integrated circuit includes a memory array having a plurality of memory cells, the method of operation comprises:

receiving block size information, wherein the block size information defines a first amount of data to be input ~~from a bus~~ in response to a write request;

receiving a first write request; and